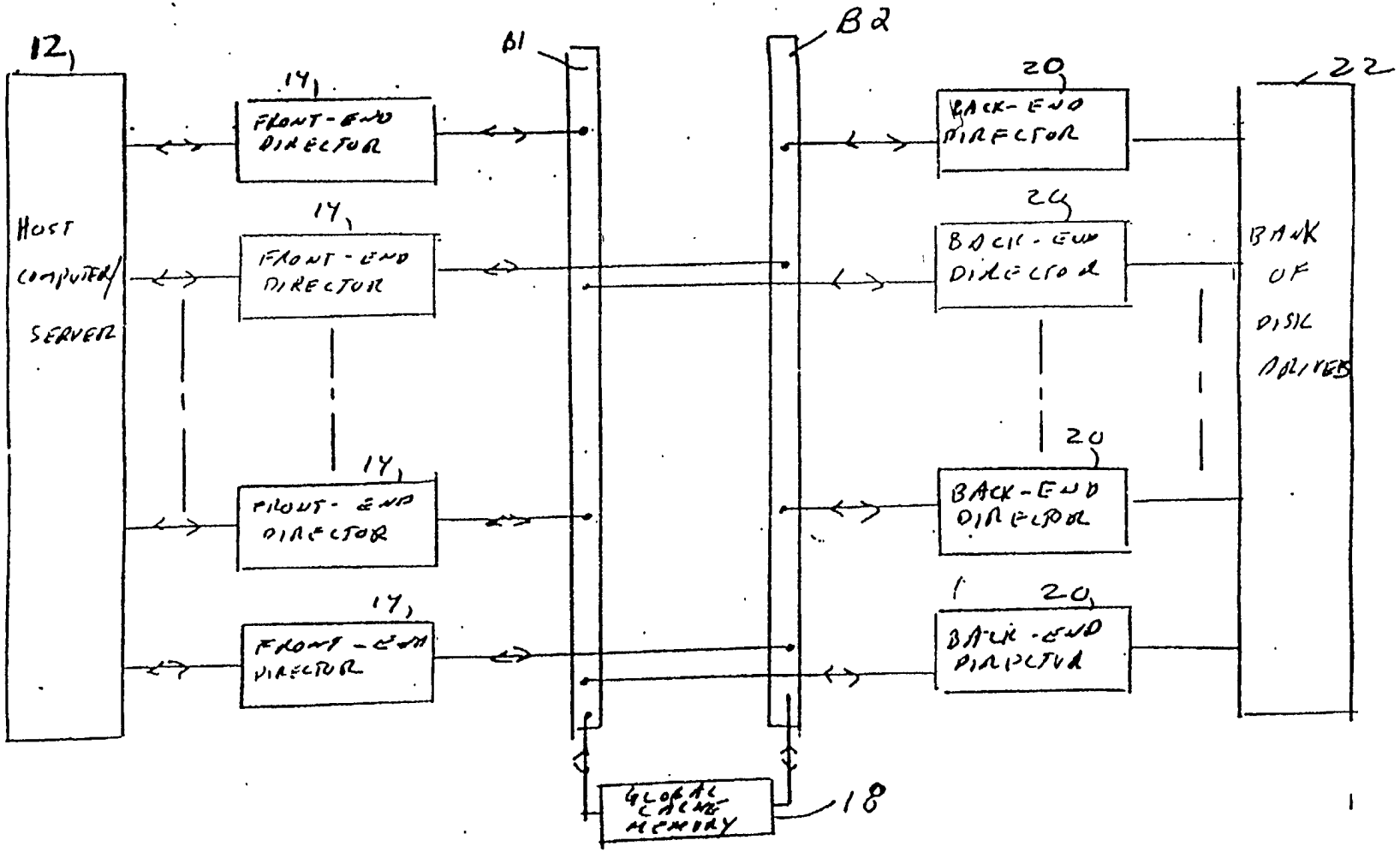
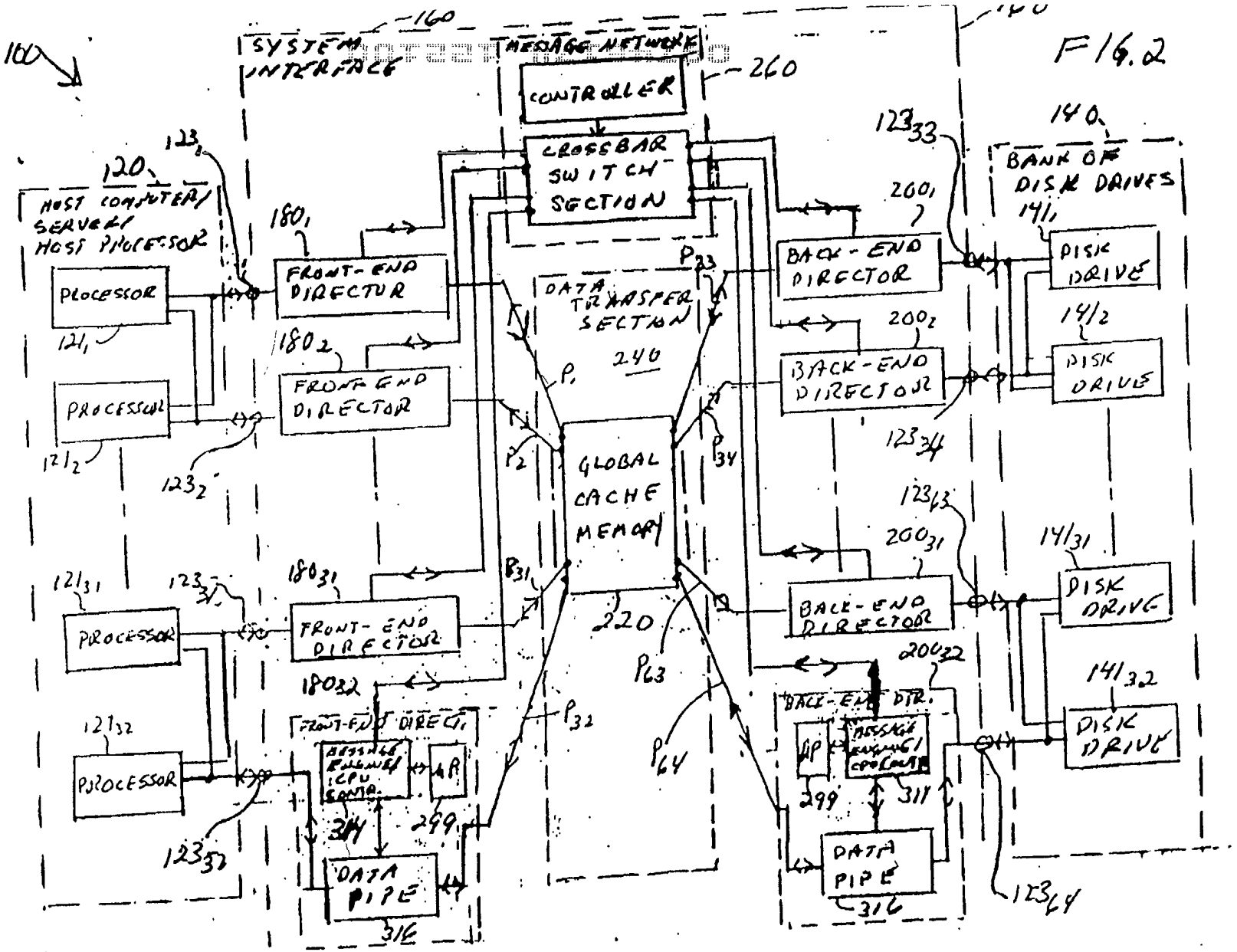
FIG. 1
PRIOR ART




100
SYSTEM INTERFACE
160
MESSAGE NETWORK
CONTROLLER
260
CROSSBAR SWITCH SECTION
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
DATA TRANSFER SECTION
240
GLOBAL CACHE MEMORY
220
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIR.
MP
MESSAGE ENGINE/ CPU CONTR.
299
311
DATA PIPE
316
DATA PIPE
316
140
BANK OF DISK DRIVES
DISK DRIVE
DISK DRIVE
DISK DRIVE
DISK DRIVE
P1
P2
P31
P32
P33
P34
P63
P64

F16.2

16 64
x4

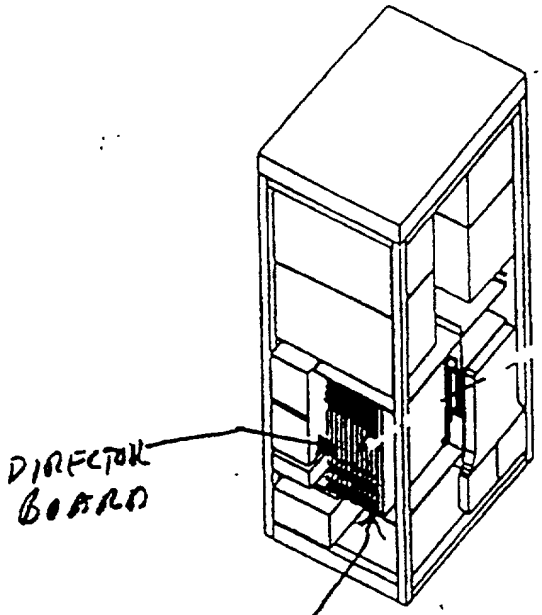
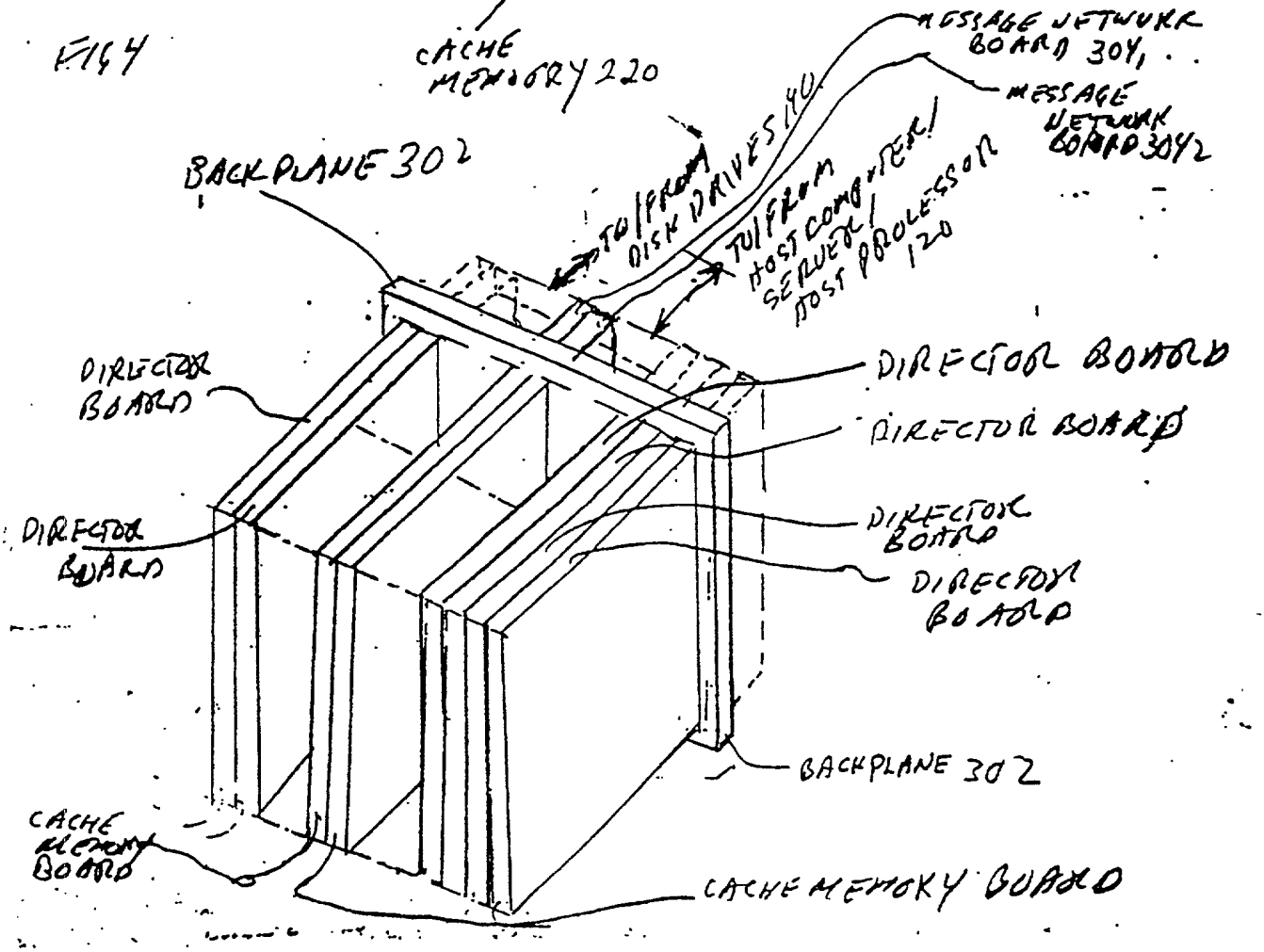

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304,
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD

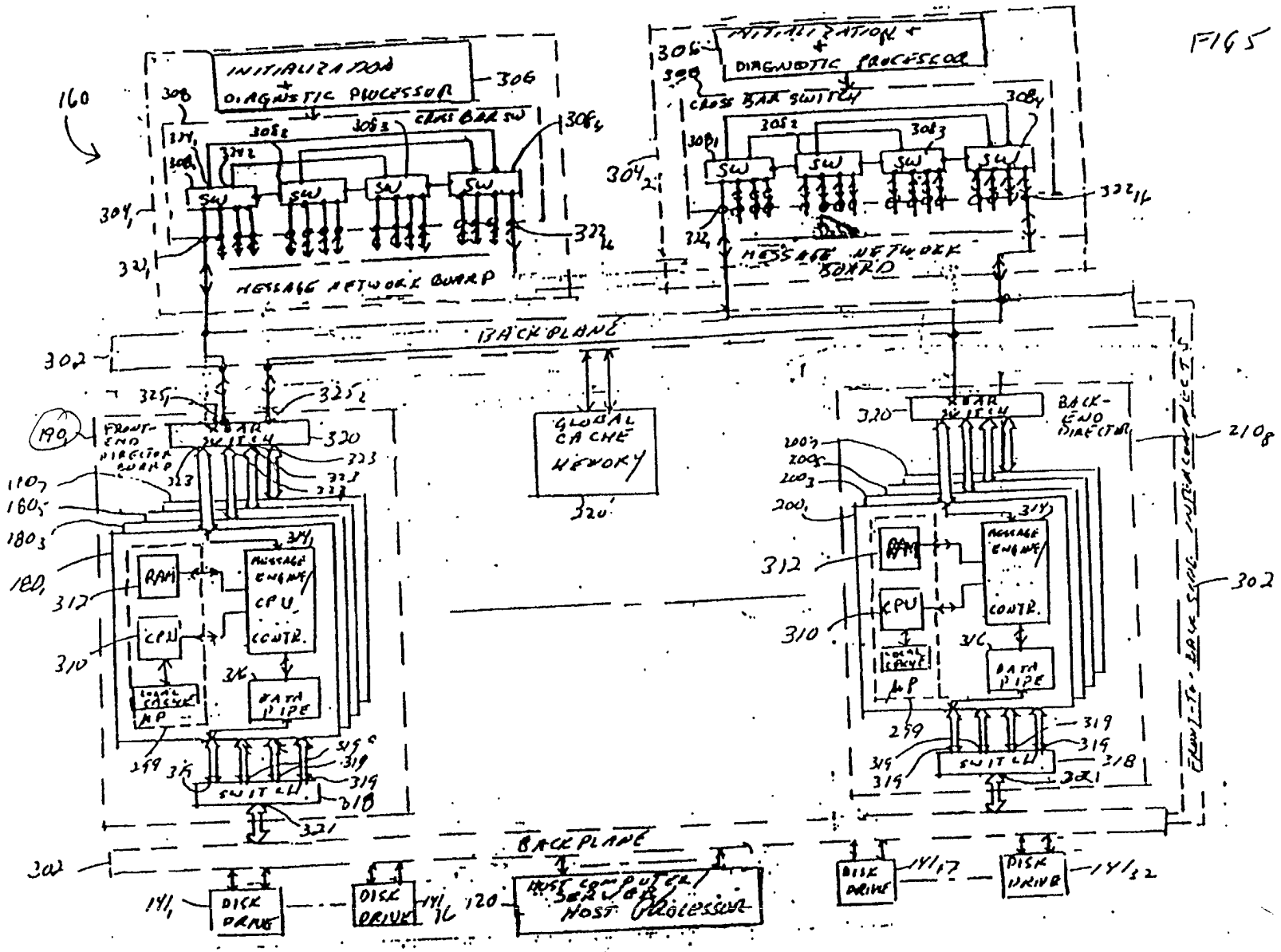

INITIALIZATION + DIAGNOSTIC PROCESSOR
CROSS BAR SW
MESSAGE NETWORK BOARD
BACKPLANE
GLOBAL CACHE MEMORY
FRONT-END DIRECTOR BOARD
BACK-END DIRECTOR
RAM
CPU
LOCAL CACHE
MP
MESSAGE ENGINE
CONTR.
DATA PIPE
SWITCH
DISK DRIVE
HOST COMPUTER OR SERVER

FIG 5

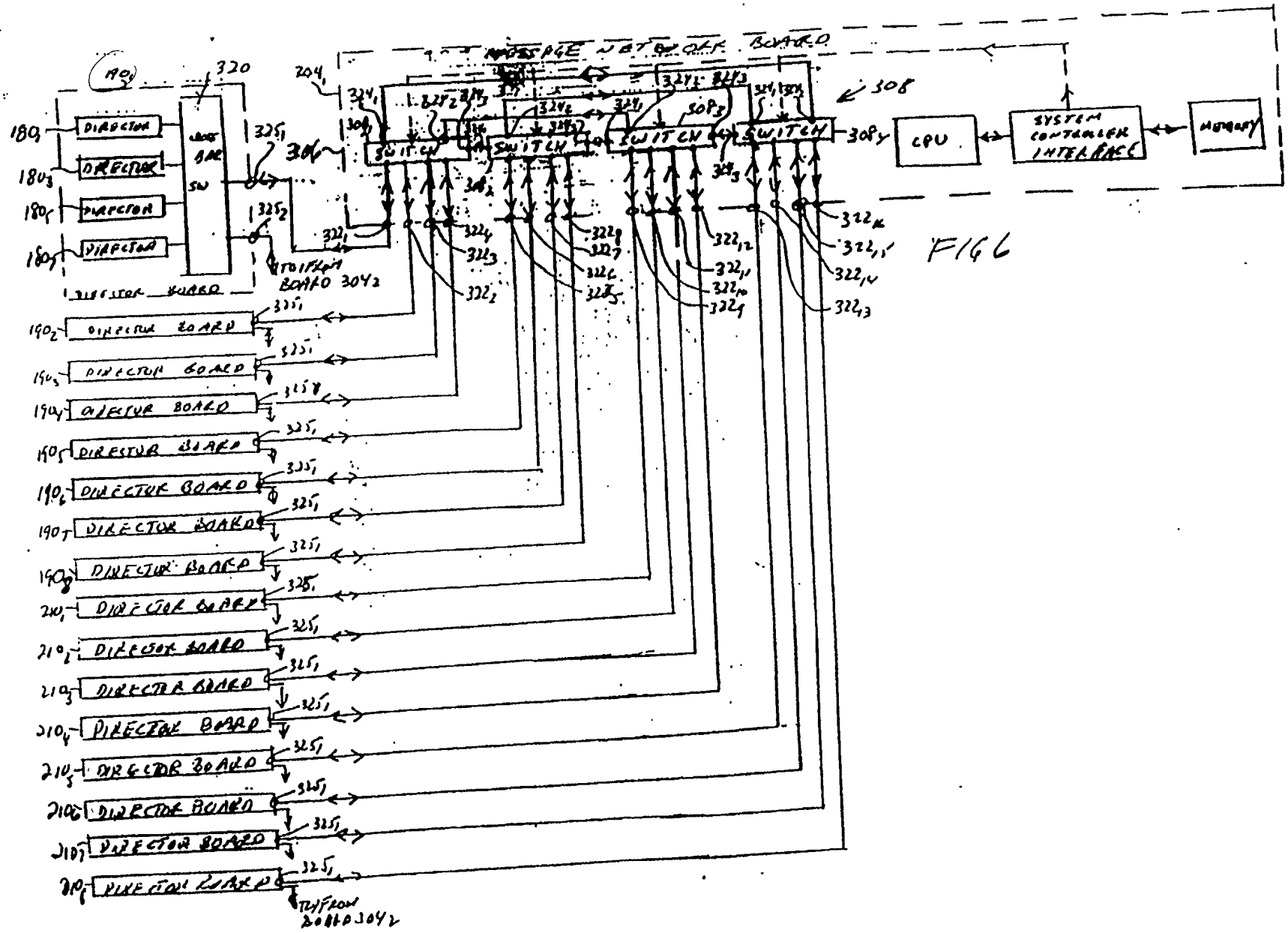
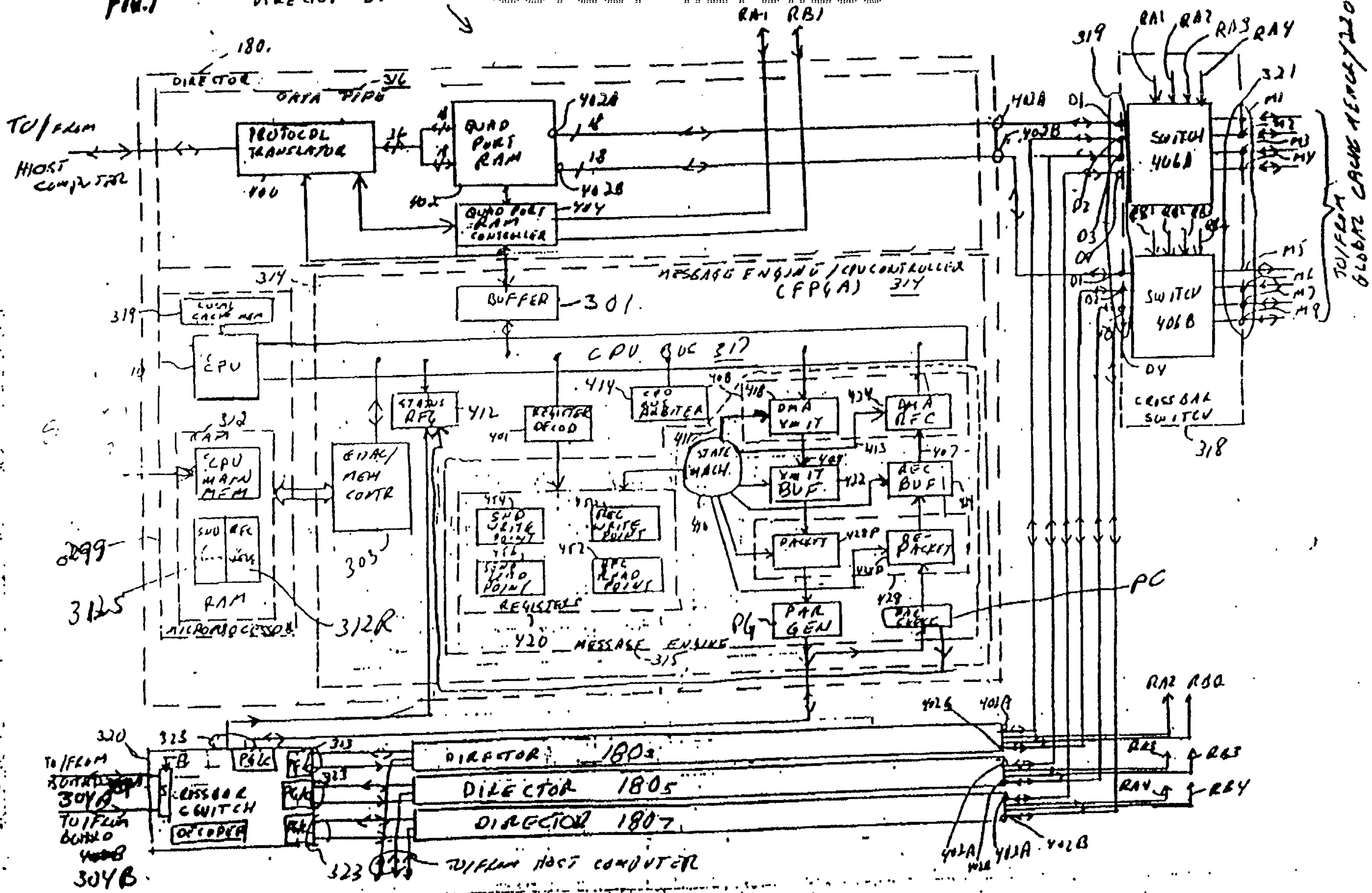

MOTHER BOARD
CPU
SYSTEM CONTROLLER INTERFACE
MEMORY
SWITCH
DIRECTOR BOARD
320
308
F16 6

FIG.7


DIRECTOR BOARD 190
180
DIRECTOR
DATA PIPE 316
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
400
QUAD PORT RAM
402
402A
402B
QUAD PORT RAM CONTROLLER
404
RA1
RB1
BUFFER 301
MESSAGE ENGINE / CPU CONTROLLER (FPGA) 314
CPU BUS 317
LOCAL CACHE MEM
319
CPU
312
CPU MAIN MEM
RAM
MICROPROCESSOR
299
312S
312R
EDAC/MEM CONTR
303
STATUS REG
412
REGISTER DECOD
401
414
CPU BUS ARBITER
DMA XMIT
DMA REC
XMIT BUF
REC BUF
STATE MACH.
PACKET
DE-PACKET
PAR GEN
PAR CHECK
PG
PC
SND WRITE POINT
REC WRITE POINT
SND READ POINT
REC READ POINT
REGISTERS
420
MESSAGE ENGINE 315
SWITCH 406A
SWITCH 406B
CROSSBAR SWITCH
318
321
D1
D2
D3
D4
M1
M2
M3
M4
M5
M6
M7
M8
RA2
RA3
RA4
TO/FROM GLOBAL CACHE MEMORY 220
DIRECTOR 1803
DIRECTOR 1805
DIRECTOR 1807
TO/FROM HOST COMPUTER
RB2
RB3
RB4
320
323
CROSSBAR SWITCH
DECODER
TO/FROM BOARD 304A
TO/FROM BOARD 304B

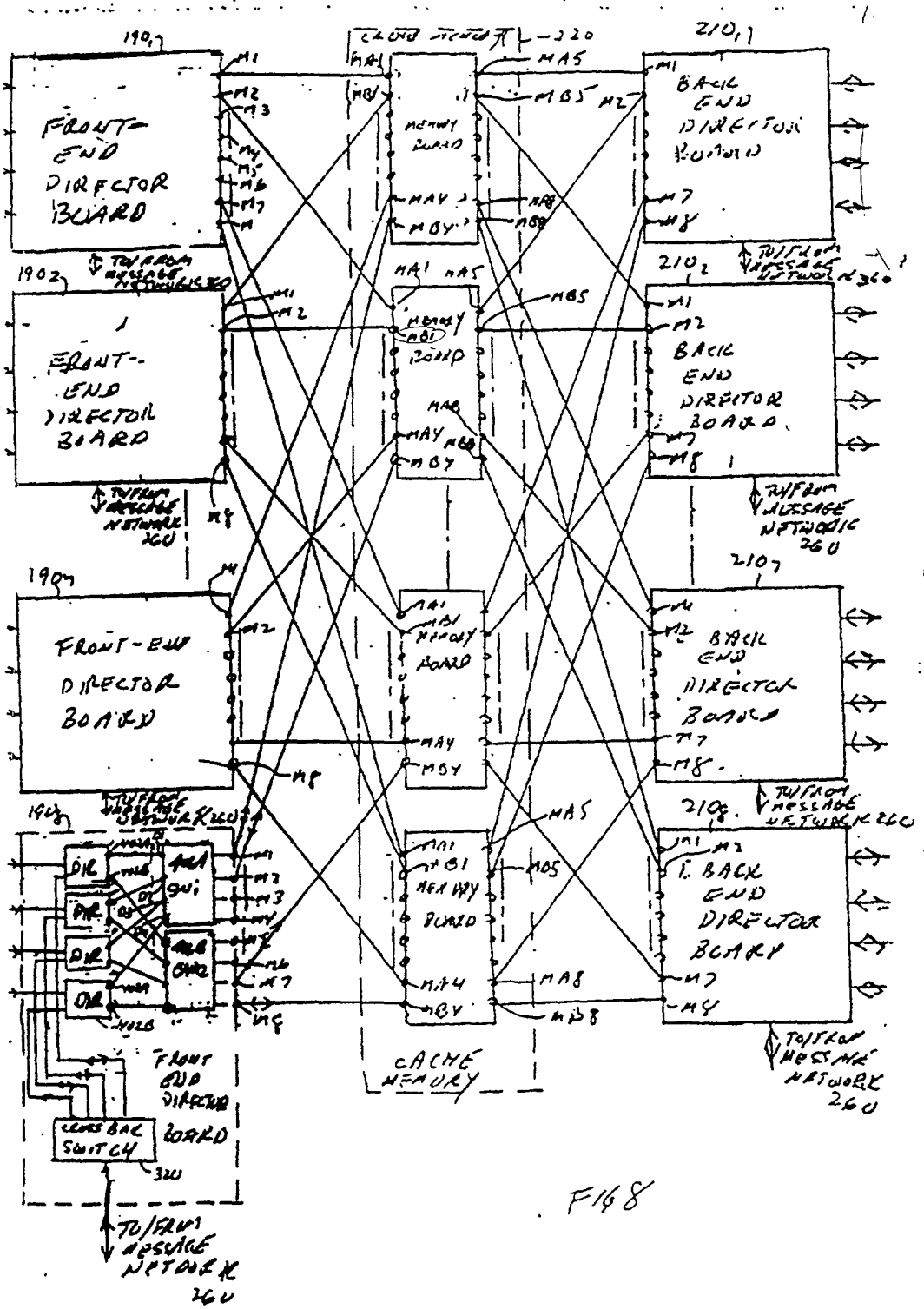
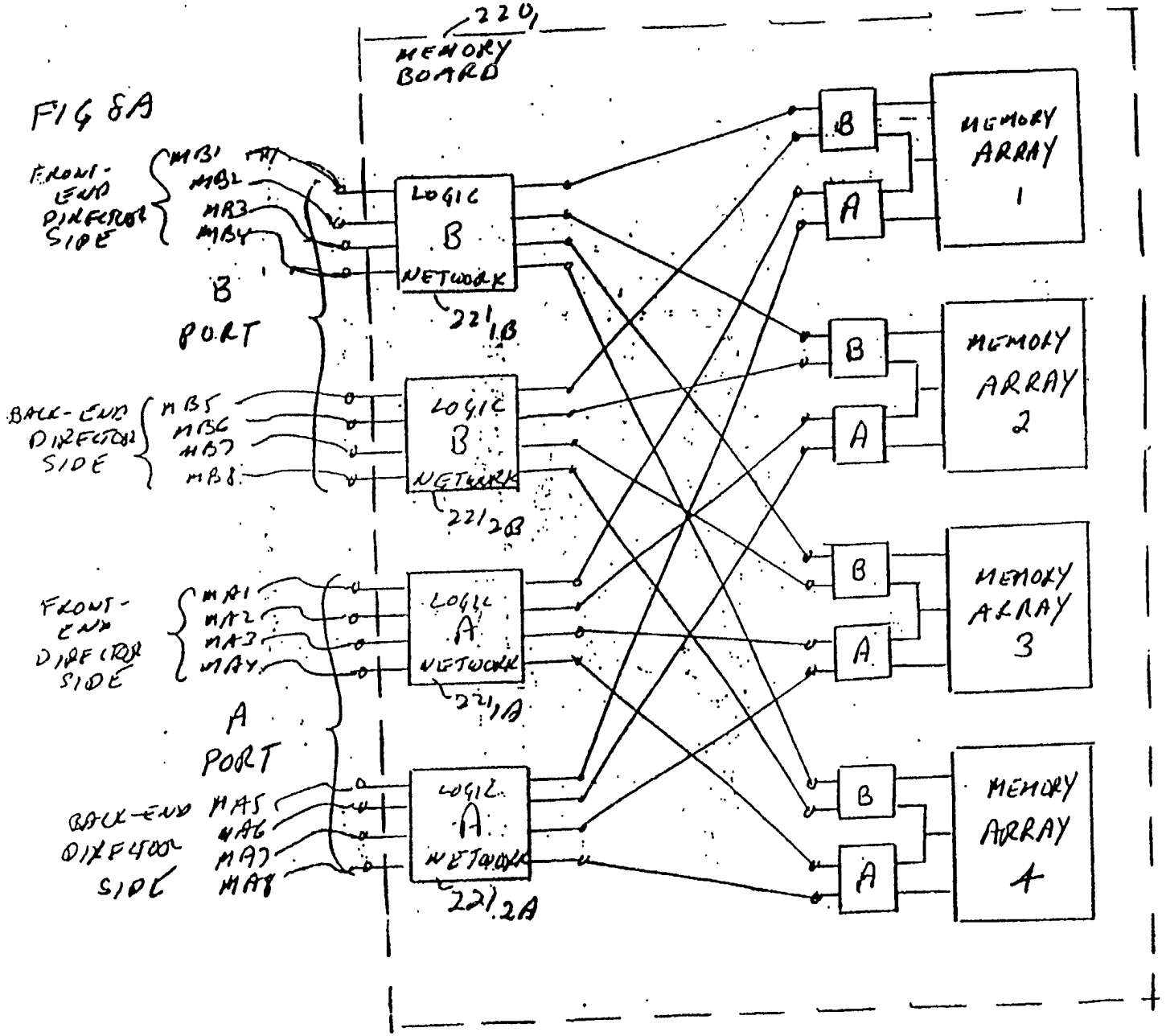

FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT END DIRECTOR BOARD
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
MEMORY BOARD
CACHE MEMORY
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
SERVICE BAC SWITCH
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260
TO/FROM MESSAGE NETWORK 260

FIG 8

FIG 8A



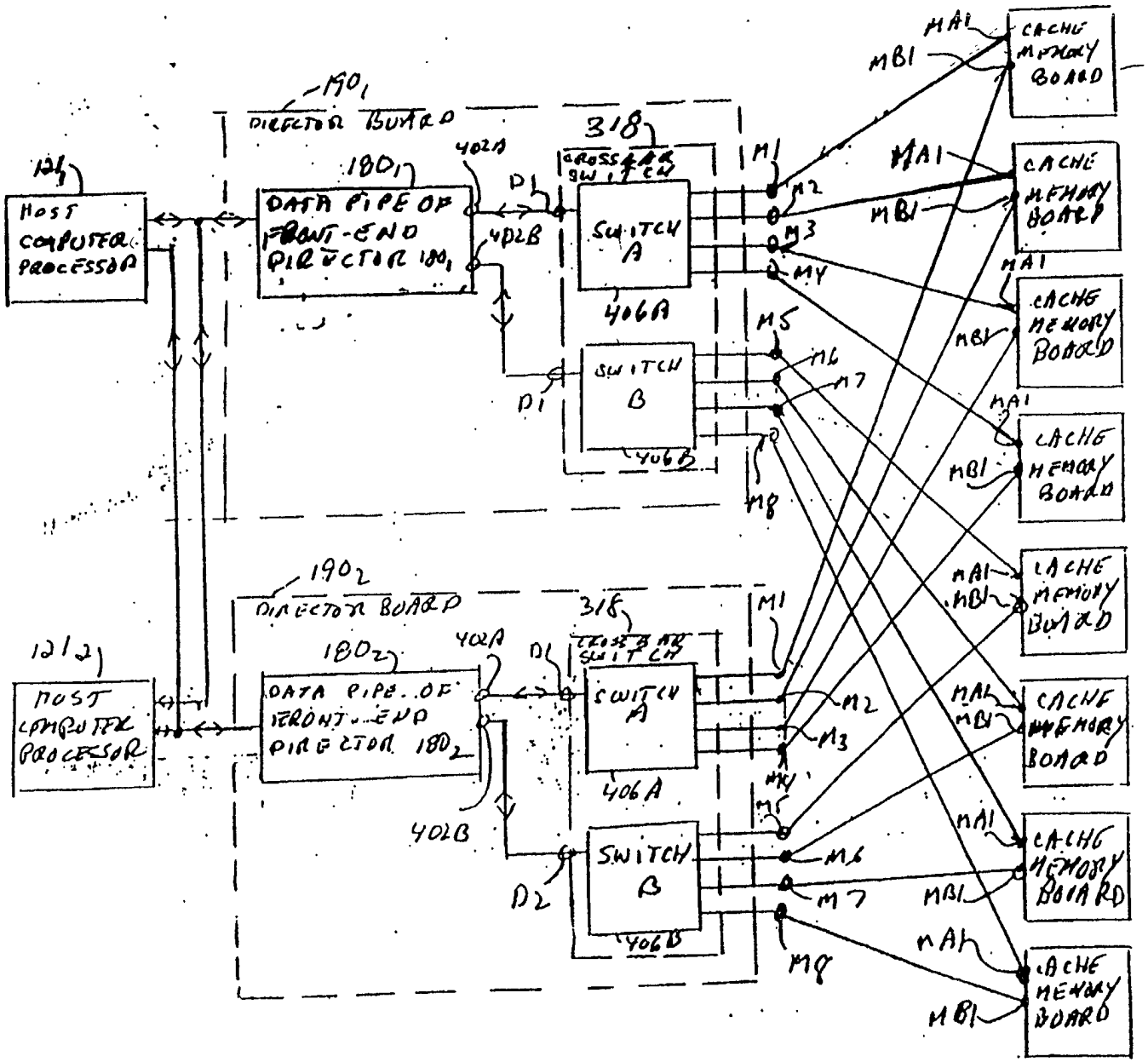

DIRECTOR BOARD
DATA PIPE OF FRONT-END DIRECTOR
HOST COMPUTER PROCESSOR
CROSS BAR SWITCH
SWITCH A
SWITCH B
CACHE MEMORY BOARD
MA1
MB1
M1
M2
M3
M4
M5
M6
M7
M8
D1
D2

FIG 8B

FIG. 9

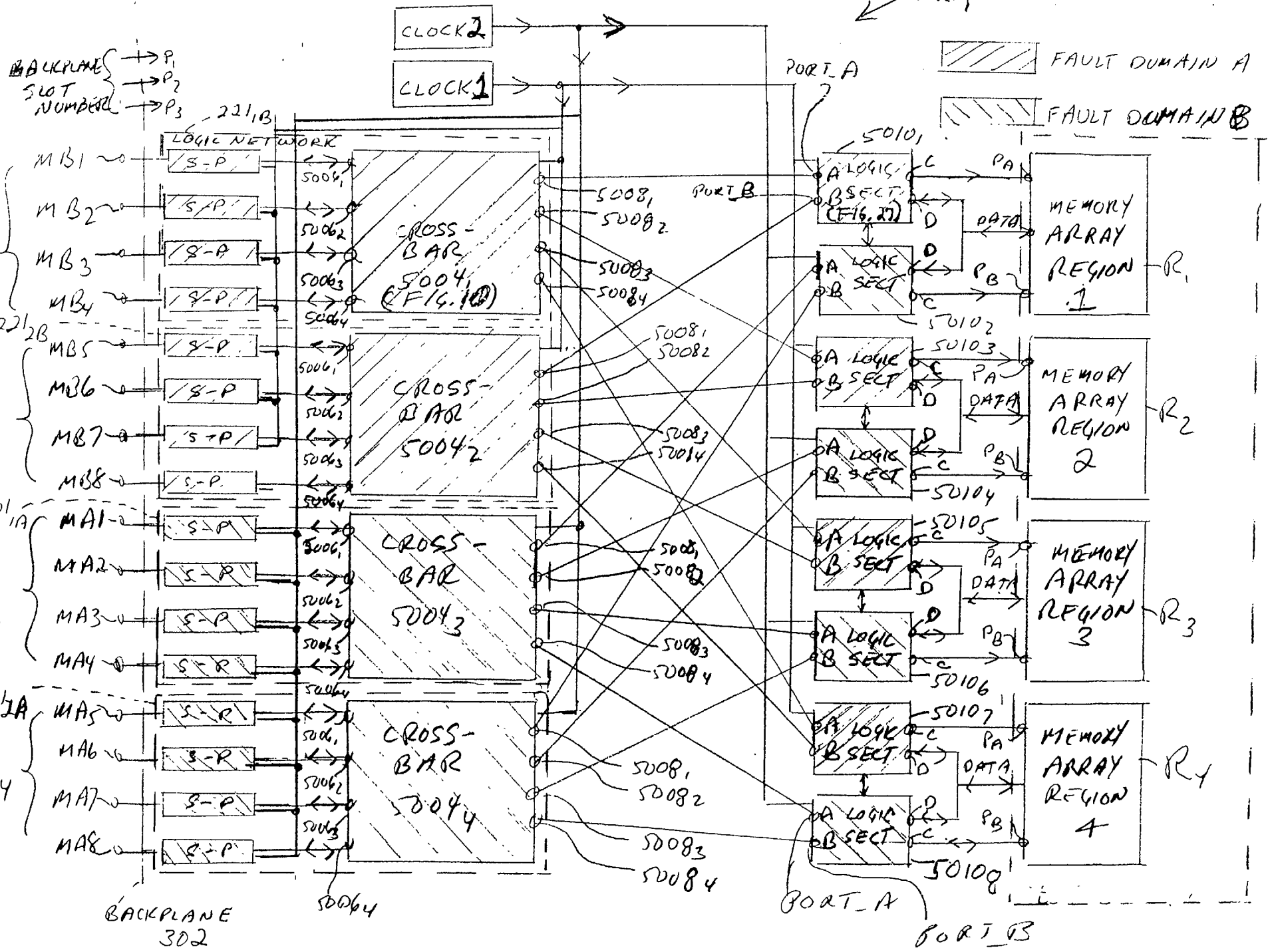
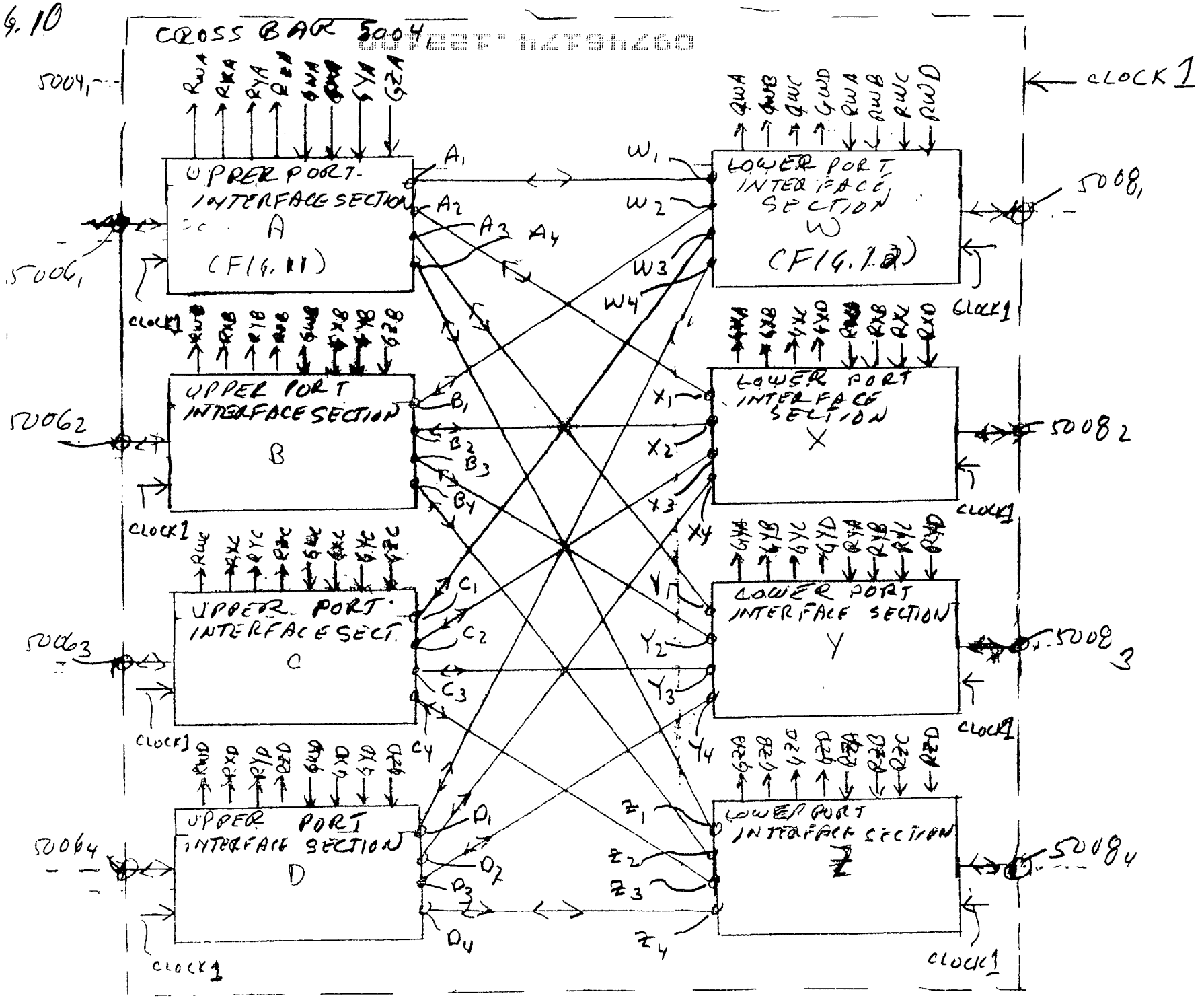

220₁
CLOCK 2
CLOCK 1
BACKPLANE SLOT NUMBERS
P1
P2
P3
221₁B
LOGIC NETWORK
MB1
MB2
MB3
MB4
S1
221₂B
MB5
MB6
MB7
MB8
S2
221₁A
MA1
MA2
MA3
MA4
S3
221₂A
MA5
MA6
MA7
MA8
S4
S-P
5006₁
5006₂
5006₃
5006₄
CROSS-BAR 5004 (FIG. 10)
CROSS-BAR 5004₂
CROSS-BAR 5004₃
CROSS-BAR 5004₄
5008₁
5008₂
5008₃
5008₄
PORT_B
PORT_A
5010₁
A LOGIC
B SECT
(FIG. 27)
C
D
DATA
PA
PB
5010₂
5010₃
5010₄
5010₅
5010₆
5010₇
5010₈
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
R1
R2
R3
R4
FAULT DOMAIN A
FAULT DOMAIN B
BACKPLANE 302
5006₄
PORT_A
PORT_B

FIG. 10


CROSS BAR 5004
5004₁
5006₁
5006₂
5006₃
5006₄
5008₁
5008₂
5008₃
5008₄
CLOCK 1
UPPER PORT INTERFACE SECTION A (FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECT. C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W (FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
A1 A2 A3 A4
B1 B2 B3 B4
C1 C2 C3 C4
D1 D2 D3 D4
W1 W2 W3 W4
X1 X2 X3 X4
Y1 Y2 Y3 Y4
Z1 Z2 Z3 Z4

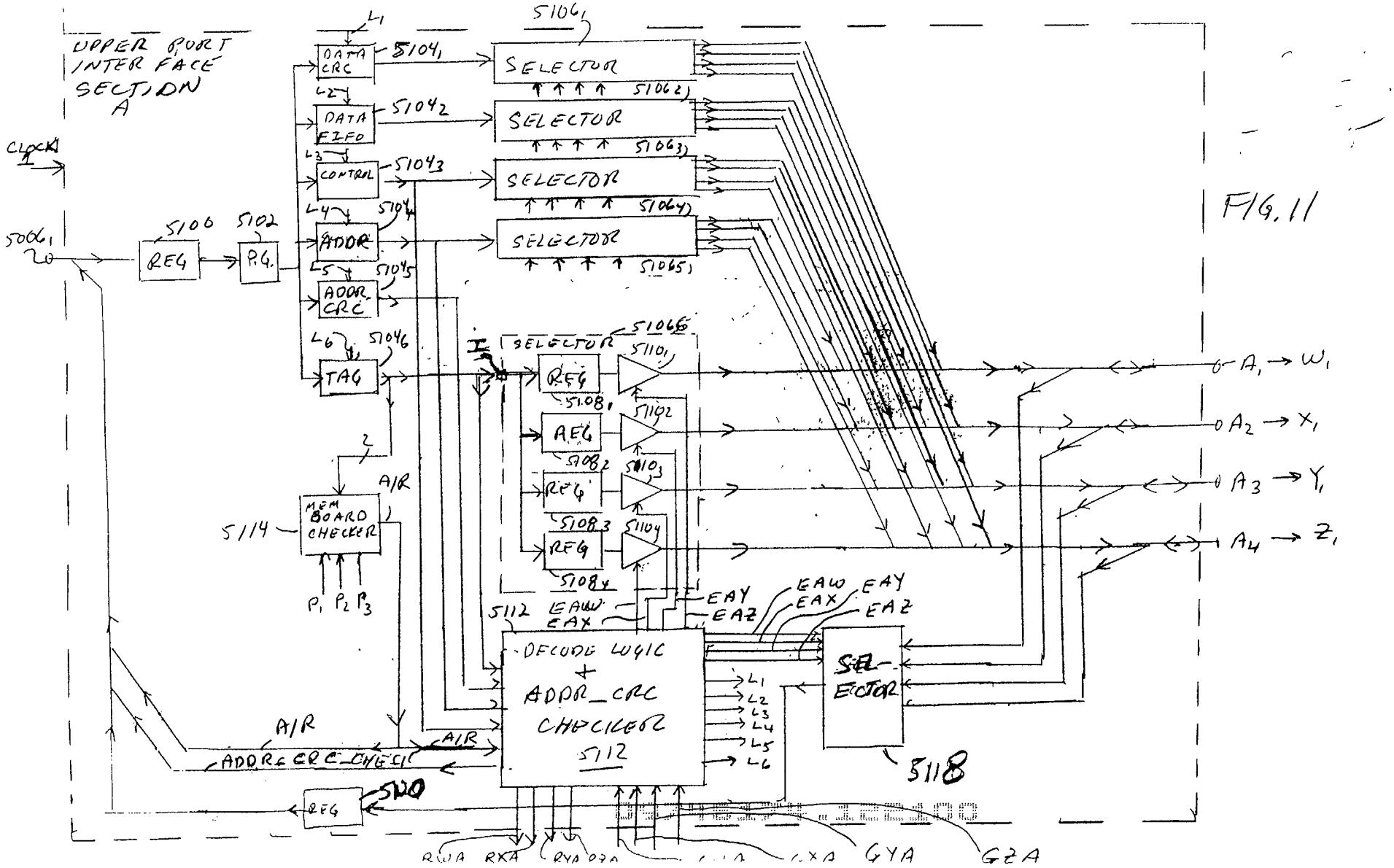
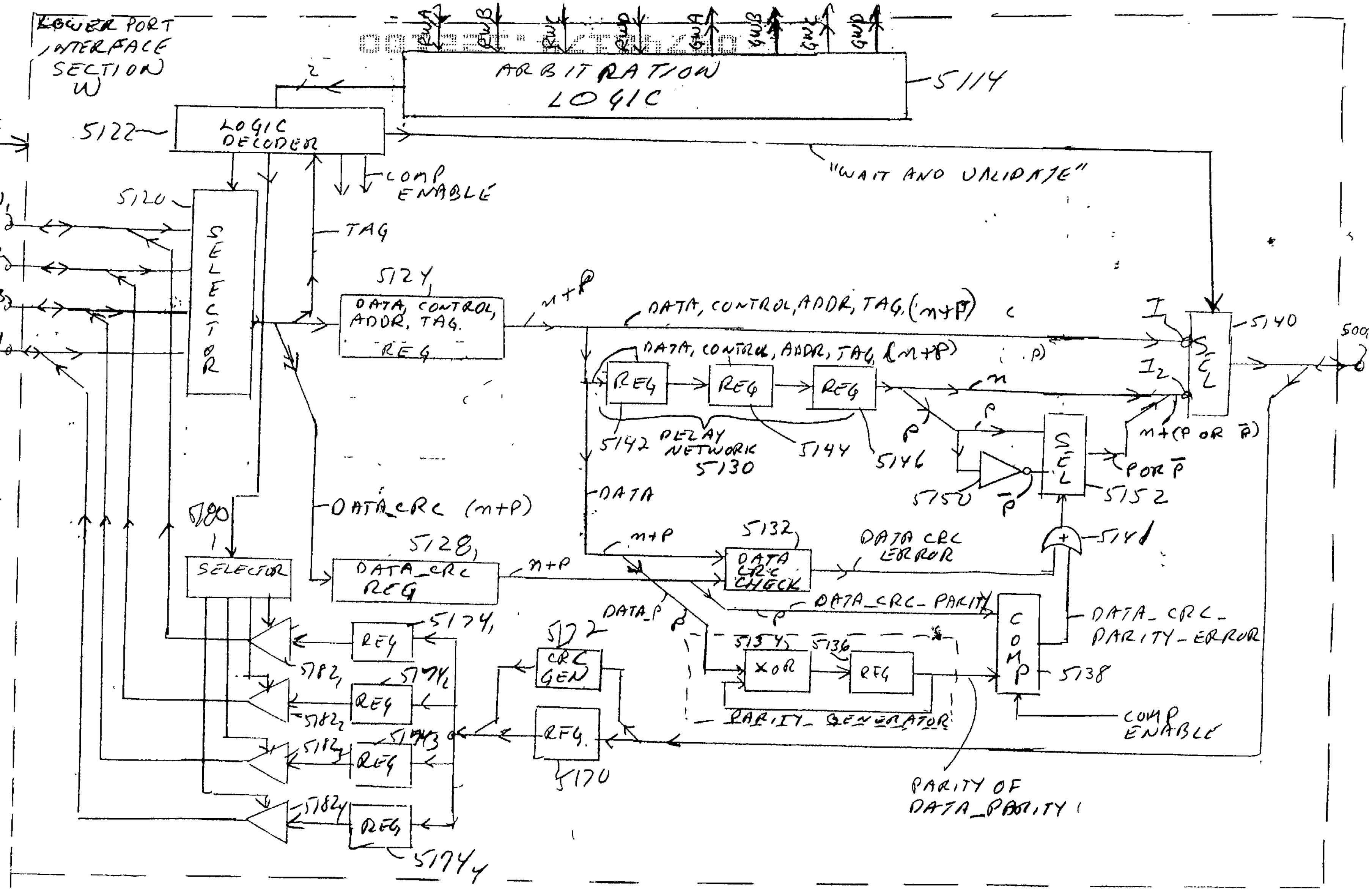

UPPER PORT INTER FACE SECTION A
CLOCK
5006
REG
5100
P.G.
5102
DATA CRC
DATA FIFO
CONTROL
ADDR
ADDR CRC
TAG
L1
L2
L3
L4
L5
L6
5104
5104
5104
5104
5104
5104
5106
SELECTOR
SELECTOR
SELECTOR
SELECTOR
5106
5106
5106
5106
SELECTOR
5106
REG
REG
REG
REG
5108
5108
5108
5108
5110
5110
5110
5110
A/R
MEM BOARD CHECKER
5114
P1 P2 P3
5112
EAW
EAX
EAY
EAZ
DECODE LOGIC + ADDR_CRC CHECKER 5112
SEL-ECTOR
5118
A1 → W1
A2 → X1
A3 → Y1
A4 → Z1
ADDR_ERR_CHECK
REG
5120
RXA
RYA
GYA
GZA

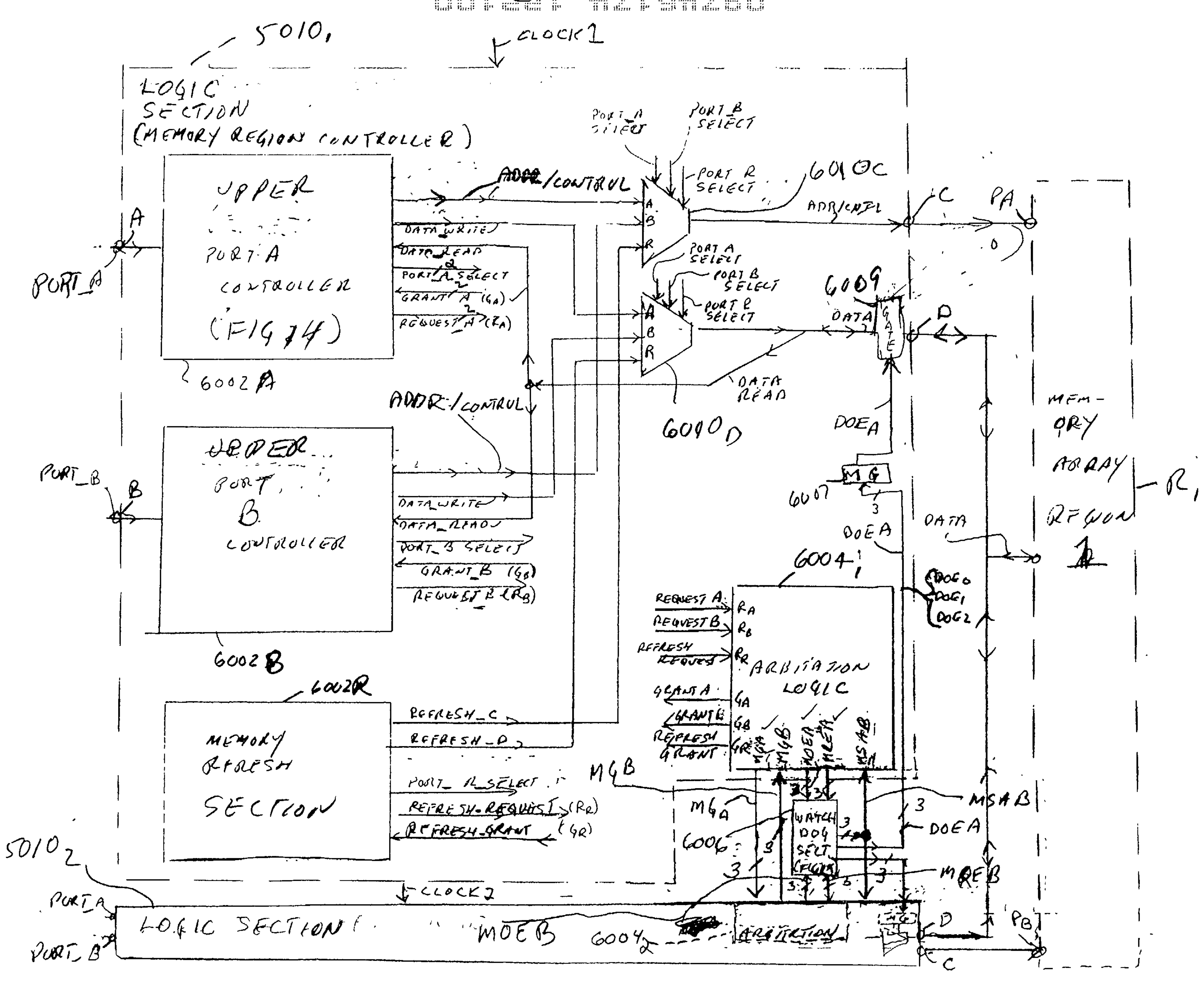
FIG. 11

FIG. 12



LOWER PORT INTERFACE SECTION W
ARBITRATION LOGIC
5114
LOGIC DECODER
5122
CLOCK 1
"WAIT AND VALIDATE"
COMP ENABLE
TAG
SELECTOR
5120
W1
W2
W3
W4
5124
DATA, CONTROL, ADDR, TAG, REG
m+p
DATA, CONTROL, ADDR, TAG, (m+p)
REG
REG
REG
5142
DELAY NETWORK 5130
5144
5146
5140
I1
I2
SEL
m+(p or p̄)
p or p̄
5150
5152
5148
DATA
DATA_CRC (m+p)
5128
DATA_CRC REG
5132
DATA CRC CHECK
DATA CRC ERROR
DATA_CRC_PARITY
DATA_CRC_PARITY_ERROR
COMP
5138
DATA_P
5134
5136
XOR
REG
PARITY GENERATOR
PARITY OF DATA_PARITY
CRC GEN
5172
REG
5170
5180
SELECTOR
5174₁
5174₂
5174₃
5174₄
5182₁
5182₂
5182₃
5182₄

FIG. 13



5010₁
CLOCK 1
LOGIC SECTION (MEMORY REGION CONTROLLER)
UPPER PORT A CONTROLLER (FIG 14)
6002A
UPPER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
6002R
PORT_A
PORT_B
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_A_SELECT
GRANT_A (GA)
REQUEST_A (RA)
GRANT_B (GB)
REQUEST_B (RB)
PORT_B SELECT
REFRESH_C
REFRESH_D
REFRESH-REQUEST (RR)
REFRESH-GRANT (GR)
PORT_A SELECT
PORT_B SELECT
PORT R SELECT
6010C
6010D
ADDR/CNTL
DATA
DATA READ
6009
GATE
DOEA
MG
6007
PA
PB
C
D
MEMORY ARRAY REGION R1
DATA
DOG0
DOG1
DOG2
6004₁
ARBITRATION LOGIC
REQUEST A
REQUEST B
REFRESH REQUEST
GRANT A
GRANT B
REFRESH GRANT
RA
RB
RR
GA
GB
GR
MGA
MGB
MOEA
MOEB
MSAB
WATCH DOG SELECT (FIG 15)
6006
MREB
5010₂
CLOCK 2
LOGIC SECTION
ARBITRATION
6004₂

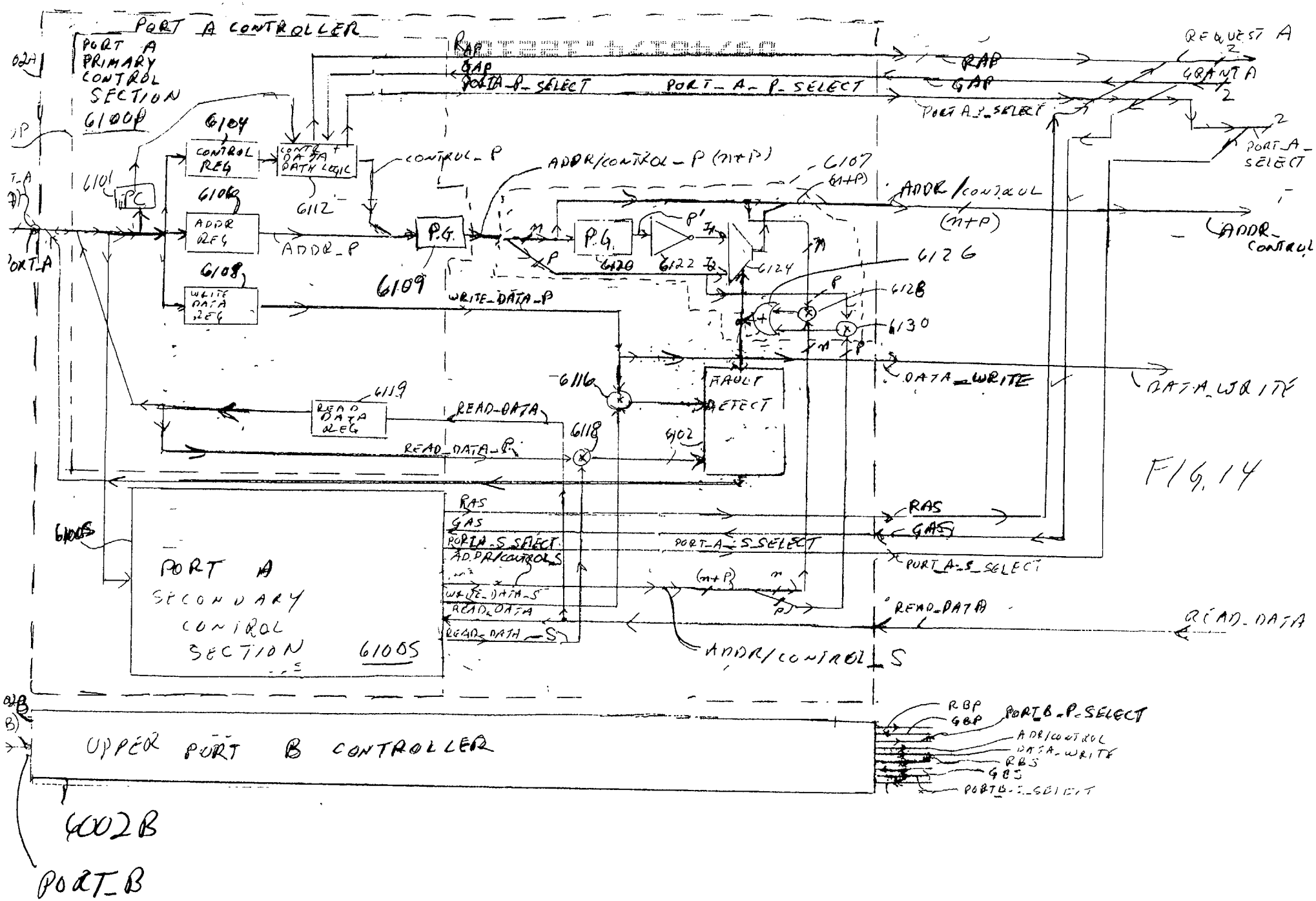
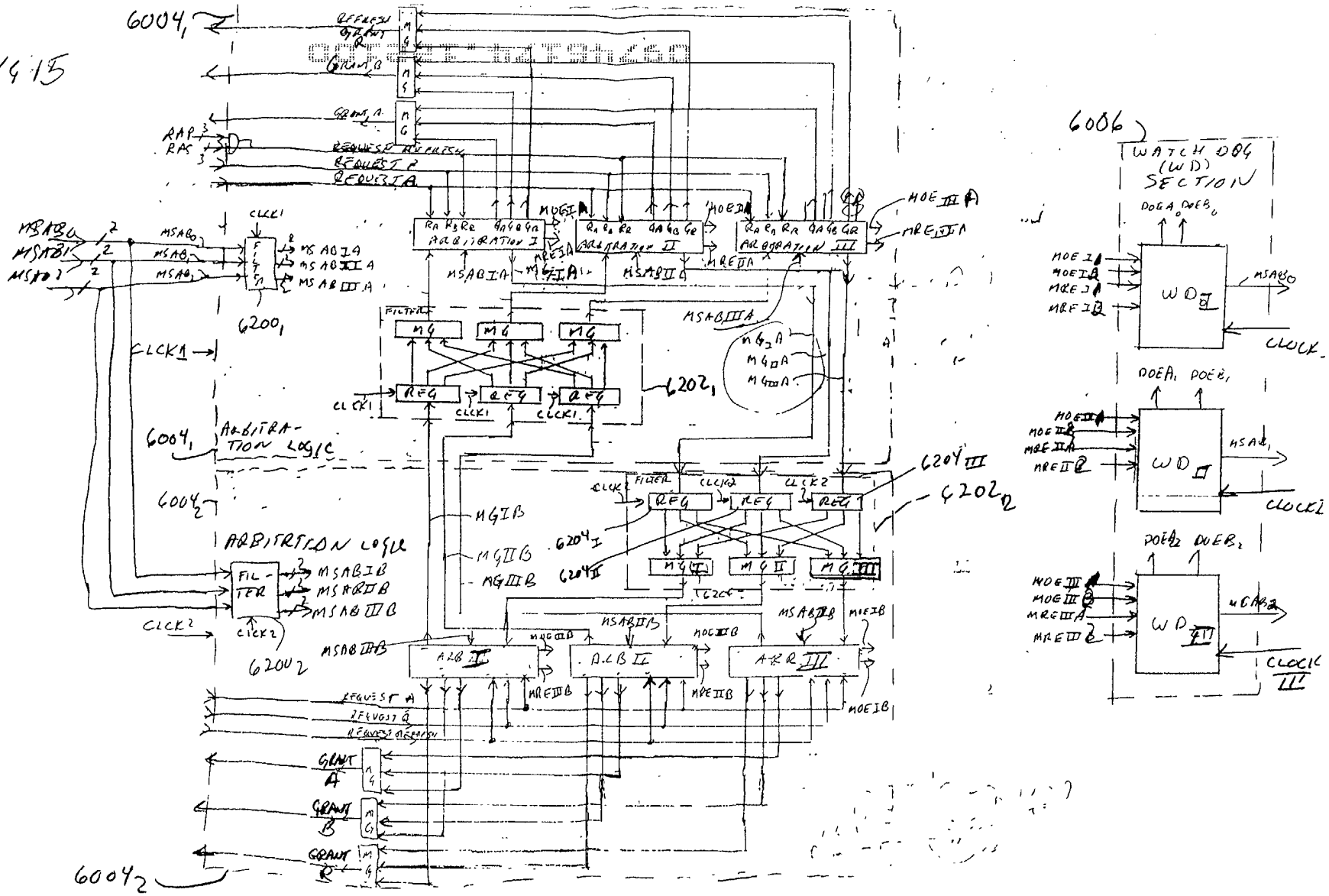

PORT A CONTROLLER
PORT A PRIMARY CONTROL SECTION
6100P
6104
CONTROL REG
CONTROL DATA PATH LOGIC
6101
PC
6106
ADDR REG
6108
WRITE DATA REG
6112
CONTROL_P
ADDR_P
6109
P.G.
ADDR/CONTROL_P (n+P)
6107
P.G.
6120
6122
6124
6126
6128
6130
ADDR/CONTROL (n+P)
ADDR_CONTROL
WRITE_DATA_P
DATA_WRITE
6116
FAULT DETECT
6119
READ DATA REG
READ_DATA
READ_DATA_P
6118
6102
RAS
GAS
PORT_A_S_SELECT
ADDR/CONTROL_S
WRITE_DATA_S
READ_DATA
READ_DATA_S
6100S
PORT A SECONDARY CONTROL SECTION
6100S
REQUEST A
GRANT A
PORT_A_P_SELECT
PORT_A_S_SELECT
RAP
GAP
RBP
GBP
PORT_B_P_SELECT
ADDR/CONTROL
DATA_WRITE
RBS
GBS
PORT_B_S_SELECT
READ_DATA
ADDR/CONTROL_S
UPPER PORT B CONTROLLER
6002B
PORT_B

FIG. 14

FIG 15


6004₁
6004₂
ARBITRATION LOGIC
ARBITRATION LOGIC
ARBITRATION I
ARBITRATION II
ARBITRATION III
FILTER
REG
CLOCK1
CLOCK2
6202₁
6202₂
6204 I
6204 II
6204 III
6200₁
6200₂
MSAB0A
MSAB1A
MSAB2A
MSAB0B
MSAB1B
MSAB2B
MGIA
MGIIA
MGIIIA
MGIB
MGIIB
MGIIIB
MOEIA
MOEIIA
MOEIIIA
MREIA
MREIIA
MREIIIA
MOEIB
MOEIIB
MOEIIIB
MREIB
MREIIB
MREIIIB
REQUEST A
REQUEST B
REQUEST R
GRANT A
GRANT B
GRANT R
RAP
RAS
6006
WATCH DOG (WD) SECTION
WD I
WD II
WD III
CLOCK
CLOCK1
CLOCK2
MSAB0
MSAB1
MSAB2
DOEA0 DOEB0
DOEA1 DOEB1
DOEA2 DOEB2
MOE I A
MOE I B
MRE I A
MRE I B
MOE II A
MOE II B
MRE II A
MRE II B
MOE III A
MOE III B
MRE III A
MRE III B

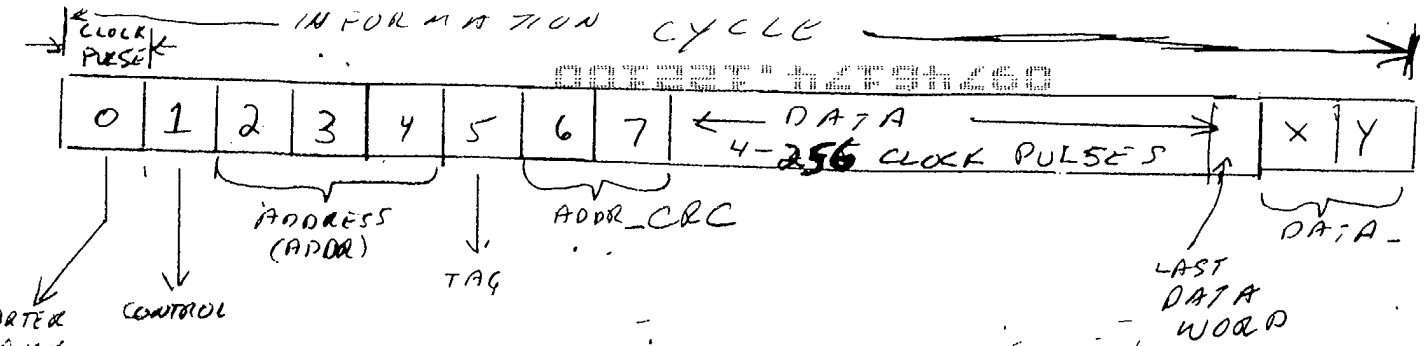


FIG. 16

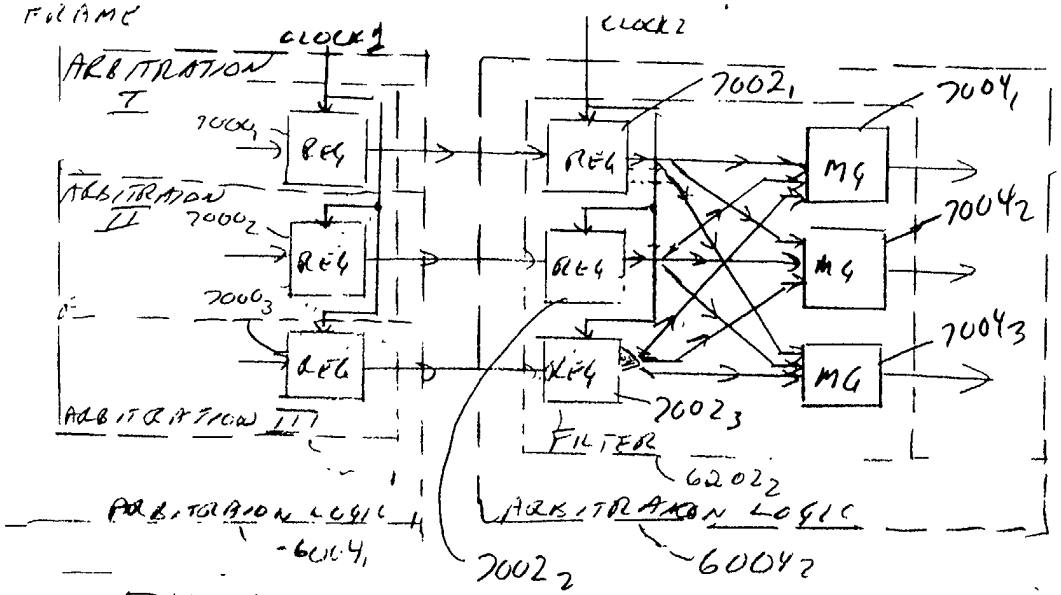


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

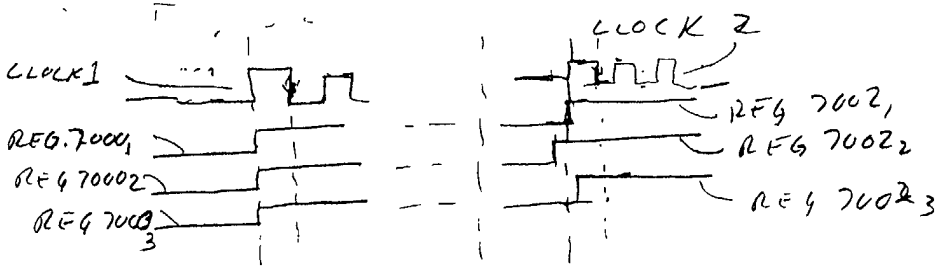
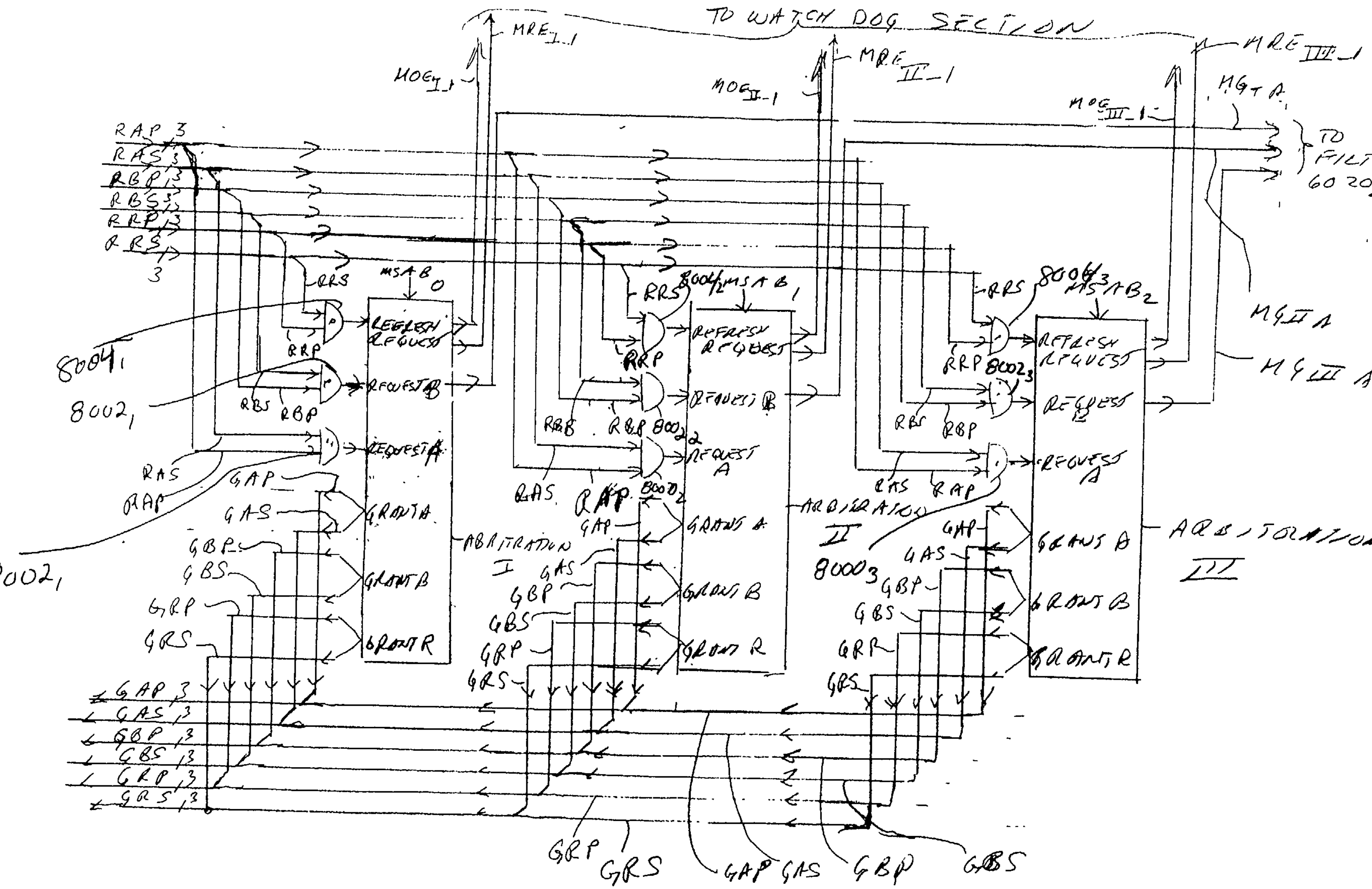


FIG. 19

FIG 2D


TO WATCH DOG SECTION
TO FILTER 6020₂
ARBITRATION I
ARBITRATION II
ARBITRATION III
REFRESH REQUEST
REQUEST B
REQUEST A
GRANT A
GRANT B
GRANT R
8004₁
8002₁
8003
MGII A
MGIII A